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Designing an Inverter using Adiabatic Logic Circuits and Power Analysis with CMOS Logic

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Abstract

Power consumption is a crucial factor in VLSI technology. In the fastest growing technologies, the circuit consumes greater power, and the circuit design is more complicated. This article describes CMOS logic circuits and presents an alternate technique to designing low-power devices. Adiabatic logic is the name given to this innovative method. This paper sheds light on the study of various logic style analyses and the development of a new low-power method for very large-scale integration. This inverter was constructed using adiabatic logic technology as well as several adiabatic strategies to minimize power dissipation. In this study, many CMOS logic styles were examined, and the Modified ECRL (MECRL) adiabatic technique was found to be the best low power consumption strategy when matched to other approaches. Tanner simulator v16was used for this investigation.

Keywords: *MECRL, Adiabatic logic, CMOS Logic, Power dissipation, PFAL, 2N-2P.*

Introduction

With the employment of several logic styles in electronic devices, power consumption can be lowered. Technological advances has prompted designers to develop new low-power circuits and has prompted researchers to investigate new logic types for circuit design. The concept also leads to the development of energy recovery logic, like adiabatic logic.

There are three forms of power dissipation: static, dynamic, and short circuit power dissipation. Several logic models can be categorized in terms of power dissipation. The logic types are implemented using a variety of low power circuits and can be used for a variety of purposes. However, there is a large power dissipation factor, and the power leakage in the circuit is observed to be greater [1]. The circuit solves the problem of power dissipation by incorporating a recycling method. The dissipated power can be recovered, and the power clock can be used once again. When contrasted to certain other logic types, adiabatic logic saves a significant amount of power [2]. An adiabatic circuit allows a few of the energy received from the power supply to be reused and reduced while switching actions are performed.

Adiabatic, as stated by a thermodynamics process, indicates that energy is not transferred with the surrounding environment, implying that no power or energy will be dissipated. Because power is not dissipated as heat energy through the resistor included in the switching operation,

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adiabatic logic is advantageous. Rather, the load capacitance conserves the power back to the supply, and the same energy (or) power is employed for the following operation.[21] The heat is preserved while the energy is regained without any losses in the system. The energy contained in load capacitors, that will be used to recycle grounded charges back to the power clock [3]. Although they have comparable capabilities in terms of creating intermediary nodes and outputs, the loads inside have been modified. Several designs prioritize one aspect of performance above others. Full adders are made in some devices from a single logical design, whereas others have many [4]. The node capacitances are charged and discharged, and only a little amount of energy is wasted and recovered via the capacitors [5].

The analysis starts with fully adiabatic gates and then expands to cover partially adiabatic circuits like 2N-2P and 2N-2N2P. SPICE simulations utilizing 0.8-µm CMOS technology validate the analytical results, as explained in [6]. In terms of power consumption, the PFAL circuit proved to be the most efficient flip-flop-based adiabatic solution [7], [8]. Thus, it has been seen that, Adiabatic CMOS circuits can be effectively used to actualize a computerized circuit configuration utilizing slowly rising and falling force clock. Either retractile course power tickers or various stage power timekeepers with memory plans can be utilized in huge circuit structure with low control utilization. The adiabatic circuit configuration can be improved by presenting ordinary power supply[19]. Further to improve the exchanging velocity of the adiabatic circuit as contrast with CMOS rationale, new adiabatic circuits with a better exchange rate can be planned. In the ECRL, because of the cross-coupled PMOS transistors, the pre-charge and recover phases give entire output swings. The device, switches off when the supply clock voltage reaches the PMOS threshold value. As a result, the recovery path linking to the clock becomes severed [9]. The style of fast low power full viper cells essentially dependent on Associate in different rationale approach has been given, which results in incredible enhancement for respects of intensity postpone metric for the arranged adders, contrasted and numerous aforesaid distributed acknowledge. The full adders planned exploitation improved rationale structure of XOR and XNOR and after that the EEAL,ECRL rationale plans, less deferral of around 3-5 ns and less control utilization of around 1-2 W, for Associate in by and large decrease of half-hour connection to the least difficult included one among the contrary adders been looked at, anyway for the most part concerning five hundredth connection to the contrary ones. Later on some work is accomplished to plan rapid low power full adders, considering adiabatic rationale structure and run new acknowledge for the constituent rationale squares (XOR/XNOR, EEAL and ECRL)[18].

Literature Survey

In [10], a simple combinational circuit 4:1 multiplexer was built utilizing several configurations of adiabatic logics. The power savings at various frequencies are evaluated to determine the efficacy of various adiabatic logic families in terms of reduced power consumption. A review on how these techniques work against a circuitry and external biases have been given in [11]. Reduce variance and decrease leakage current in adiabatic logic circuits to preserve energy-

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efficient sub-threshold operation [12], [13]. Advanced structures have experienced emotional changes in the course of recent decades |moving from chips that contained a huge number of gadgets to the present chips that may contain over a billion transistors. The activity of the advanced circuit fashioner has developed with the chips, moving from upgrading and approving entryways, to chipping away at useful units, to now planning total frameworks. While the advancement in computerized configuration has obviously been huge, handling present and future framework issues and power difficulties will prompt noteworthy further development. We anticipate seeing reports of these computerized circuit configuration propels throughout the following two years of the gathering [14].

This paper surveys the fundamental portrayal of adiabatic rationale families. Adiabatic circuits utilized in numerous high frequencies application with low control dissemination. It was likewise seen that the completely adiabatic circuits diminish the power utilization significantly but they are exceptionally mind boggling to structure and even though the incompletely adiabatic circuits are not as proficient as completely adiabatic circuits as far as power utilization yet they lessen the circuit intricacy and moderate the power. So we can say that in part adiabatic circuits are reasonable trade off between the power utilization. It is conceivable further to diminish the spillage control by consolidating dynamic and adiabatic rationale, when contrasted and static rationale. The rationale family favors a high recurrence transistor plan and produces great outcomes with more precision and low spillage. The power dispersal is diminished significantly while utilizing the new idea [15].

This paper surveys the adiabatic rationale circuits and some significant adiabatic rationale families have been depicted and thought about for their viability as far as decreased power dispersal when contrasted with customary CMOS rationale circuits. Of all the adiabatic rationale families analyzed, positive input adiabatic rationale (PFAL) demonstrates least control utilization rather than 2N-2N2P rationale family and ECRL rationale family. So as to diminish control dissemination, we saw that the rationale exchanging ought not be immediate but rather should be steady. As the journey for ultralow power circuit plans continues expanding, these improved circuit advances would demonstrate to help serve the need. Additionally, watching the readings from various tables shows that for a specific rationale circuit, postpone remains almost steady at a specific recurrence as dc voltage is fluctuated from0.1V to 0.3 V [16]. Over voltage-scaled static CMOS, Boost Logic achieves significant energy savings over a considerably wider frequency range than already proven in charge-recovery literature. The energy overhead of the suggested power-gating method was evaluated in depth, and an analytical model for power-gating adiabatic sequential circuits was built [16], [17].

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Inverter implementation using ECRL

The inverter circuit has been implemented using the Proposed Modified ECRL logic and other conventional logic circuits in this article using Mentor Graphics v16.0 tool. An implementation of the inverter circuit is performed using PFAL, DFAL, CAL,SCRL, 2N-2P and Quasi logics, and they have all been compared with the Proposed Modified ECRL logic, which yielded impressive outcomes.

Proposed Modified ECRL (MECRL)

The MECRL is calculated using pairs of pull down devices (NMOS) and the PMOS device. It is the most important idea in the recharge and evaluation process. Because of the cross coupled PMOS transistors, the pre-charge and recover phases give entire output swings. The device, however, switches off when the supply clock voltage reaches the PMOS threshold value. Fig. 1 illustrates this point through the proposed Modified ECRL inverter circuitry.

This suggested circuit is built around an adiabatic amplifier. P1, P2 P3 and voltage source below Q1 and Q2 forms the latch. The logic circuits Q1 and Q2 form a transmission gate by being in parallel with P1 and P2. Voltage source 1 (V1) is the single phase split level sinusoidal power supplies used in this circuit.

As a result, the recovery path that connects to the clock becomes disconnected. In our study, the ECRL has a sinusoidal clocked input voltage with four phases for each cycle. Wait, examine, hold, and recover are the four options. Fig. 2 shows the operation phases of the MECRL circuit.[20]

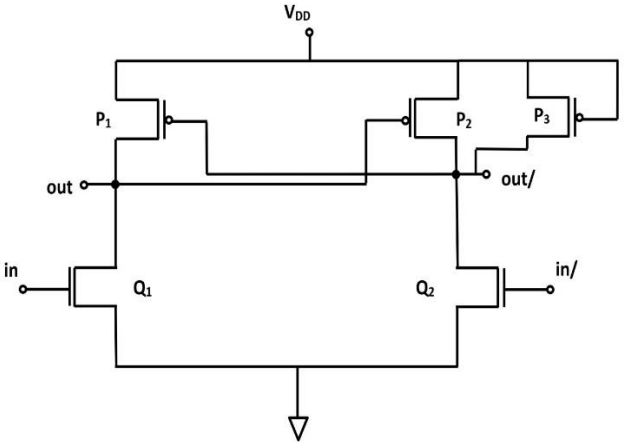

Fig. 1.Proposed Modified ECRL circuit

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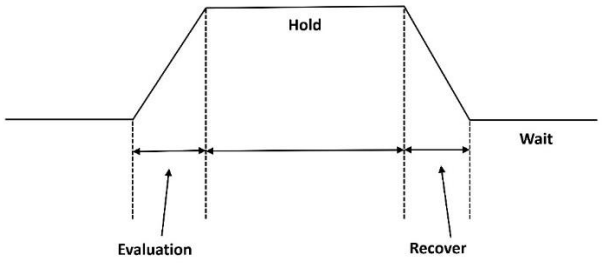

Fig. 2. Different phases of ECRL operation

An additional PMOS is placed parallel to P1 andP2, as well as an additional NMOS is connected in series to Q1 and Q2, such that these transistors facilitate load capacitance and decrease power consumption. The two basic steps of the circuit operation are *evaluation* and *hold*. V1 swings up and the voltage source below Q1 and Q2 (V3) swings down during the *evaluation* phase, and V3 swings up and V1 swings down during the *hold* phase. Assume that during the *evaluation* phase, input (in) is high and input (in/) is low; during this period, Q1 is conducting and output (out)follows the power supply V1, and P1 is turned on by output (out), lowering charging resistance. The charge stored on the load capacitances flows back to the power source through P1 during the *hold* phase.

Because it is a quasi-adiabatic technique, where some energy is returned to the source, there is a minor loss of energy in the logic due to a small difference in voltage between the source and drain. Due to the impossibility of obtaining full adiabatic processes, quasi-adiabatic approaches have recently acquired popularity. Through a series connection of the resistance and load capacitance placed in the PMOS network, the energy dissipated can be evaluated using the following formulation: [4]

$$E_{dis} = \left[\frac{RC_L}{T}\right] C_L V_{DD}^2 \qquad (1)$$

Here C_L is the load capacitance, T is the charging time.

In the beginning, the *in* signal is high and the *in/*signal is low. The supply clock climbs from 0 to V_{DD} at the start of a cycle, while *out* remains at ground. This activates Q2 and causes the *out/* to follow the supply clock through P1. The *out* and *out/* holds valid logic levels when the supply clock reaches V_{DD}. These values are kept during the *hold* phase and are also utilized as inputs for the next stage's evaluation. After the *hold* phase, the supply clock falls to the ground, and the energy is returned to the clock, allowing the charge to be recovered.

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Outcome comparison and graphical analysis

The inverter circuit is developed using the proposed MECRL technique. In order to prove the efficiency of the proposed logic, this circuit has also been implemented using several conventional logics such as PFAL, DFAL, CAL, SCRL, 2N-2P and Quasi. Through the above-addressed methodologies, the MECRL has proven to achieve better voltages and lesser power dissipations. Tanner EDA simulations are used to explore the effect of parameter modifications on energy consumption for the two logic families in a CMOS logic circuit. The simulations are done at the 130 nm technology node.

Adiabatic implementations of Inverter

The inverter circuit has been implemented using different conventional logic methodologies and their performance is compared to the proposed implementation using MECRL. The following shows the inverter architecture implementations of various logics using Tanner EDA tool.

PFAL

Two NMOS and two PMOS logic chips are used to create it. In the same way that ECRL is controlled by NMOS devices, PFAL is controlled by NMOS devices that are coupled in parallel with PMOS devices [1]. Fig. 3 shows the fundamental circuitry of the PFAL architecture.

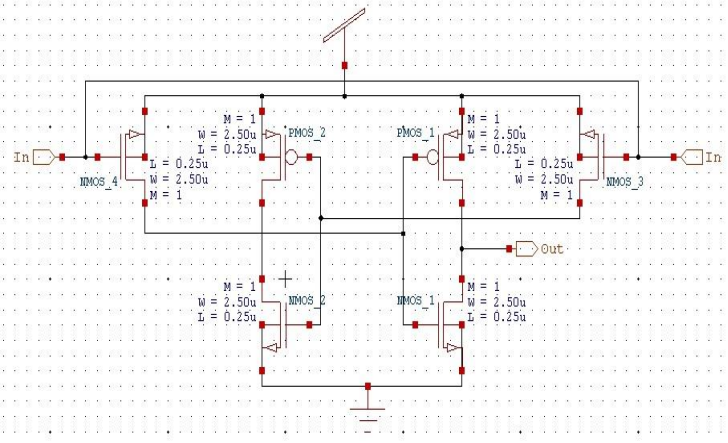

Fig. 3. PFAL inverter circuit implemented using Tanner EDA.

A PFAL circuit comprises of an adiabatic amplifier, a latch containing two NMOS and PMOS each, which eliminates decay in logic level at the output nodes. For realizing logic functions, two n-trees are used. Both positive as well as negative outputs are produced by this logic family.

DFAL

Two clock power supplies with symmetrical and asymmetrical logic are employed in this technology. Circuit functioning is divided into evaluation and hold phases based on the clock

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power [2]. One clock pulse is dedicated to the assessment, while the other is idle. Fig. 4 shows the fundamental circuitry of the DFAL architecture.

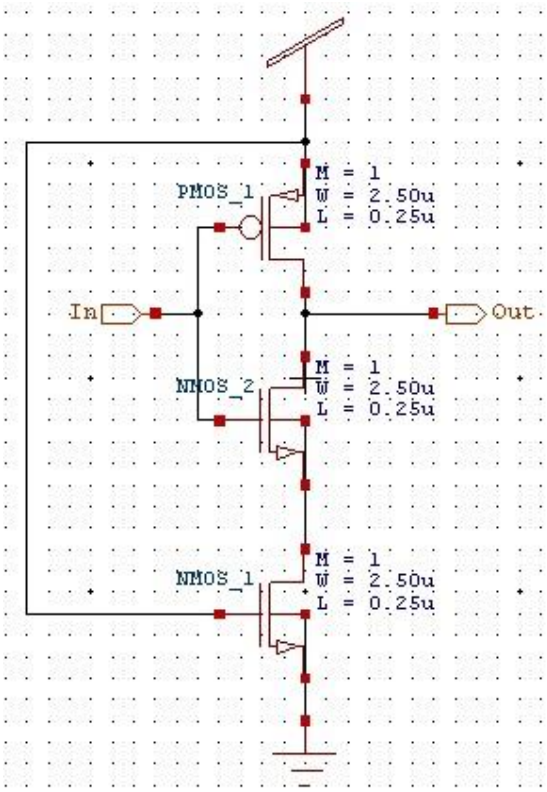

Fig. 4. DFAL inverter circuit implemented using Tanner EDA.

The DFAL diagram looks like static CMOS logic, yet the circuit functions in an adiabatic way. The discharging diode is replaced by a NMOS transistor in the pull down network close to the PMOS. The turning ON and OFF of this transistor is controlled by the power clock. The power dissipation caused by this ON resistance (of PMOS) is substantially less than the power dissipation caused by diode threshold voltage drop. PMOS also recycles charges from the output node, allowing for further recovery of adiabatic losses.

CAL

Some other technique is clocked CMOS Adiabatic logic (CAL), that is powered by a single-phase power clock in adiabatic mode and a dc power supply in non-adiabatic mode [16]. Fig. 5 shows the fundamental circuitry of the CAL architecture. In a recovery mode without consuming energy that is compatible with regular CMOS logic, can be powered by a DC power supply.

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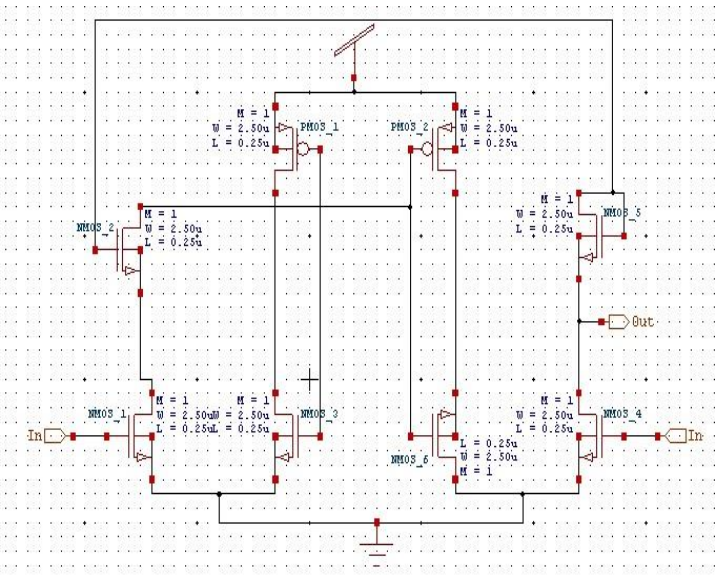

Fig. 5. CAL inverter circuit implemented using Tanner EDA.

SCRL

It doesn't require dual rail input. Supplying voltage to V_{DD} determines the logic function of SCRL. When output is enabled, the voltage level of the device is raised to $V_{DD}/2$ [14]. Fig. 6 shows the fundamental circuitry of the SCRL architecture.

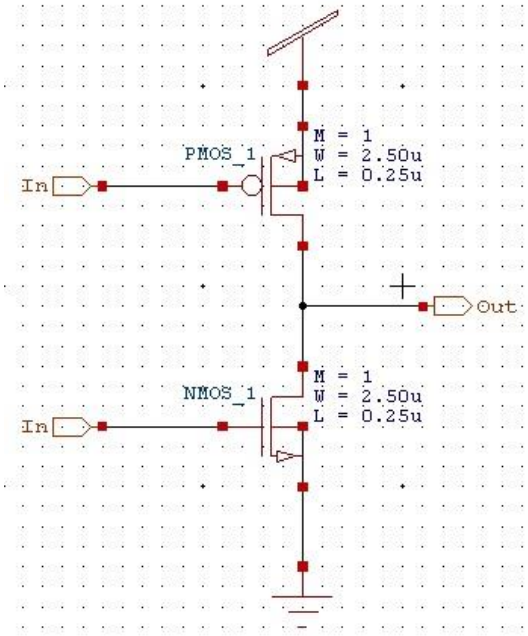

Fig. 6. SCRL inverter circuit implemented using Tanner EDA.

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2N-2P

It is built on the differential logic style of function. This moniker refers to two NMOS and two PMOS devices. This circuit is made up of cross-coupled PMOS devices, with positive and negative polarity inputs for each NMOS device [2].Fig. 7 shows the fundamental circuitry of the 2N-2P architecture.

The inputs are low, the outputs are complementary (one high, the other low), and the power supply is ramping down during the RESET phase. The power supply is kept low during the WAIT (second) phase, keeping the outputs low (which is required for the following logical gate, which is delayed by a quarter cycle, to conduct its RESET phase), and the inputs are evaluated. The power supply ramps up in the EVALUATE (third) phase, and the outputs evaluate to a complimentary state.

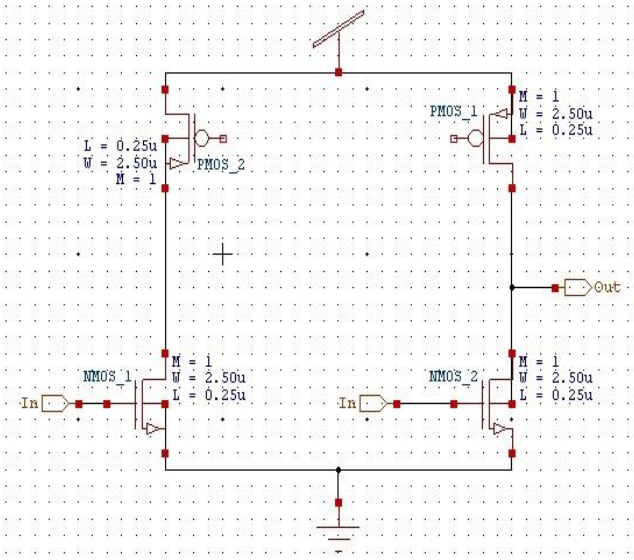

Fig. 7. 2N-2P inverter circuit implemented using Tanner EDA.

Quasi

It's adiabatic logic to a degree. It provides dc power to the circuit, similar to a CMOS inverter [2]. Fig. 8 shows the fundamental circuitry of the Quasi inverter architecture. The output nodes will not be charging and discharging at the same time per clock cycle. Only when the input signal changes does the output node need to switch. Additionally, as contrasted to previously existing adiabatic circuits such as the 2N2P, SCRL, PFAL, and others, the utilization of the sinusoidal power clock signal makes it energy efficient. In respect of maximum operating frequency and minimum voltage of operation, it's the Quasi Static Energy Recovery Logic (QSERL). The static energy recovery circuits can be used to simulate a 8 bit carry look ahead adder (CLA) and compare their energy efficiency to static CMOS logic [13].

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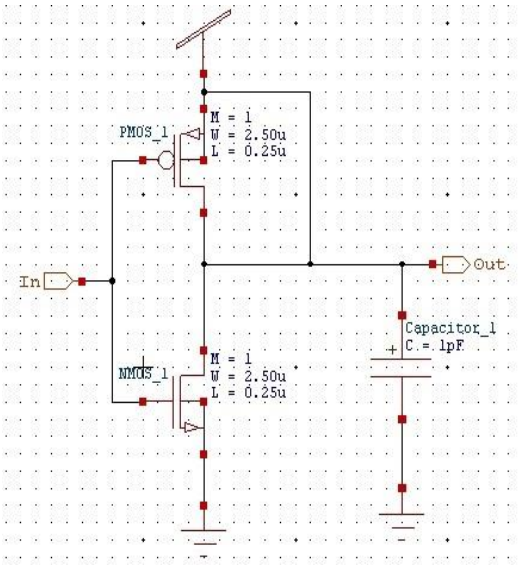

Fig. 8. Quasi inverter circuit implemented using Tanner EDA.

Proposed Modified ECRL implementation

The results of the proposed RCA circuit in MECRL technology were simulated in Tanner EDA tool using 130 nm technology. Tanner EDA tool Software was used to simulate the result of an MECRL complete adder circuit utilizing 130nm technology.

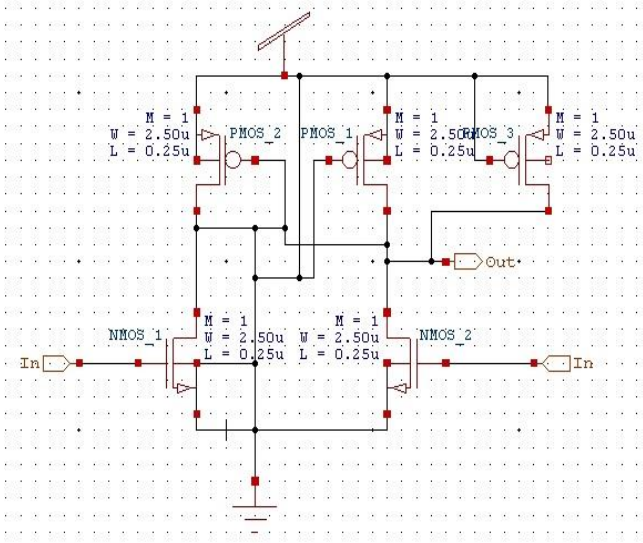

Fig. 9. Proposed Modified ECRL inverter circuit implemented using Tanner EDA.

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When a, b, and c are all 0, the resultant sum is "0," and Cout is "0." When a = 1, b = 1, and c = 1, the resultant sum is "1," and Cout is"1." The Power Dissipation obtained from the procedure is 7.783 µW. Fig. 9shows a schematic representation in the Tanner EDA tool.

The output received from the Tanner EDA tool displays real and inverted inputs, producing outputs in a similar manner. In the beginning, the *in* signal is high and the *in/* signal is low. The supply clock climbs from 0 to V_{DD} at the start of a cycle, while *out* remains at ground. This activates Q2 and causes the *out/*to follow the supply clock through P1.

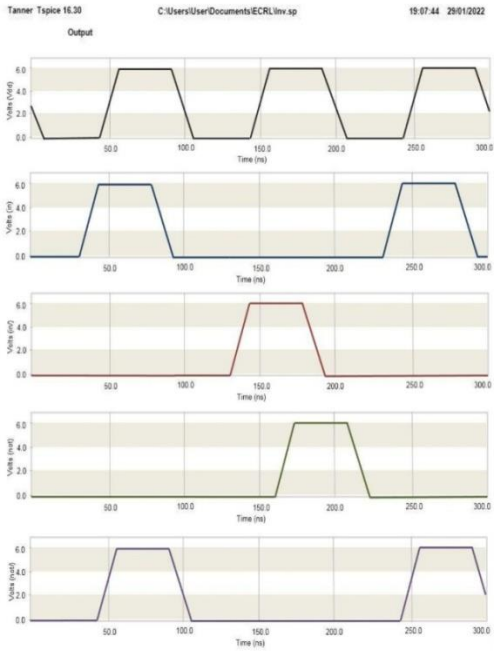

Fig. 10. Tanner EDA simulated waveform of inverter circuit designed using MECRL.

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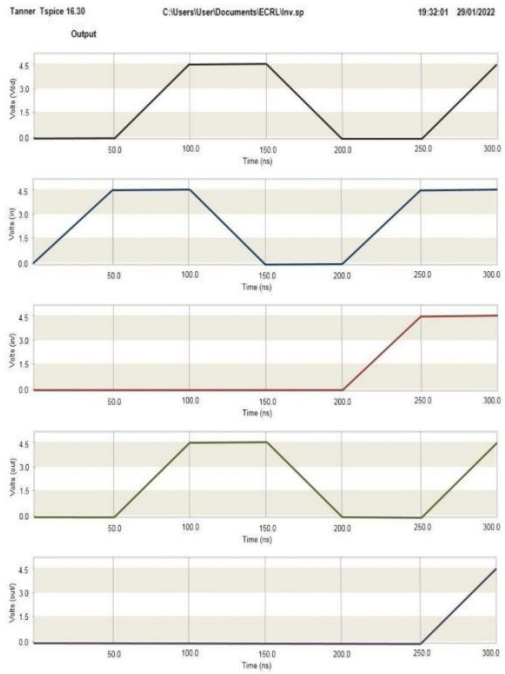

Fig. 11. Tanner EDA simulated waveform of inverter circuit designed using 2N-2P.

The *out* and *out/*holds valid logic levels when the supply clock reaches V_{DD}. These values are kept during the *hold* phase and are also utilized as inputs for the next stage's evaluation. After the *hold* phase, the supply clock falls to the ground, and the energy is returned to the clock, allowing the charge tube recovered. Fig. 10 displays the output characteristics of the inverter circuit using MECRL logic, achieving a high output voltage of 6V.

A comparison has been made between the above outcome and another logic. The implemented 2N-2P design shows a different waveform at a much lower voltage value, i.e. 4.5 V. Fig. 11 displays the outcomes of the inverter circuit developed using 2N-2P logic. MECRL yields a higher voltage value as compared to the 2N-2P logic.

Frequency variation

The energy dissipation per cycle versus switching frequency of the MECRL compared with adiabatic logic families, like CMOS and PFAL is shown in Fig. 12.It can be shown that the behavior is no longer adiabatic at high frequencies, and hence the energy dissipation increases.

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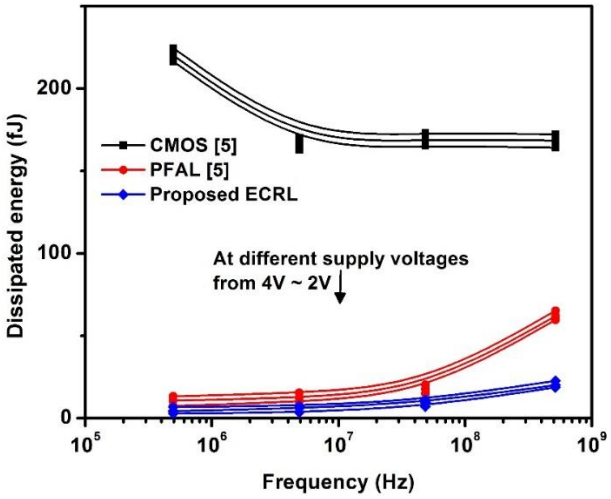

Fig. 12. Energy dissipated with respect to frequency at different supply voltages. Load capacitance kept at 20 fF.

Due to the leakage currents of the transistors, the dissipation energy both for CMOS and adiabatic logic will rise at low frequencies. Load capacitance of 20 fF is considered with increasing supply voltage.

Capacitance Variation

The energy dissipation per cycle versus load capacitance of the inverter with MECRL compares with adiabatic logic families, like CMOS and PFAL is depicted in Fig.13.

The figure illustrates that over a wide range of load capacitances, adiabatic logic families save more energy than CMOS logic.

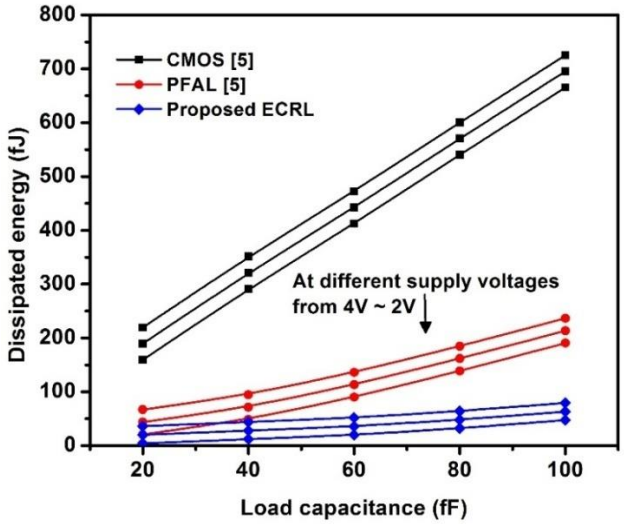

Fig. 13. Energy dissipated with respect to load capacitance at diffirent supply voltages. Operating frequency kept at 100 MHz.

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Power consumption

The MECRL logic has also been implemented using the inverter circuit andresulted in reduced power consumption in the range of micro watts (μW). Fig. 14 shows the power consumption of the proposed MECRL circuitas compared to inverter implementation using other contemporary adiabaticlogic families.

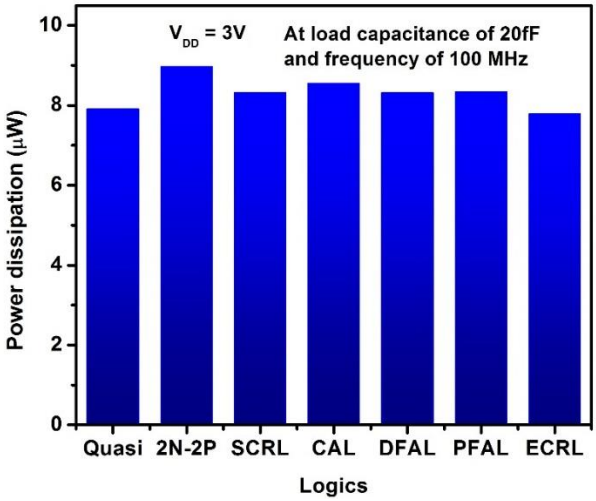

Fig. 14.Power consumption of the proposed MECRL circuit when compared with inverterimplementations using other conventional adiabatic logic families.

Table 1 compares various transistors and logic circuits with their corresponding power dissipations.

Table 1. Comparison of different transistors and power dissipation

S. No.	Inverter designing logic	Transistors required	Power dissipation (μW)
1.	PFAL	6	8.388
2.	DFAL	3	8.673
3.	CAL	8	8.552
4.	SCRL	2	8.315
5.	2N-2P	4	8.973
6.	Quasi	2	7.91
7.	Proposed MECRL	4	7.783

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Conclusion

Various adiabatic strategies have been adopted in the CMOS logic type, according to the findings of the study. It has been demonstrated that lowpower circuits have a high level of efficiency. It not only cuts power but alsoboosts speed in many circuits. When contrasted to other adiabatic approaches, MECRL appears to be a good low-power technology. The proposed inverter circuit designed using MECRL produced high amplitude in the range to 6V, much higher compared to conventional logic implementation like 2N-2P. A low energy consumption of 53 fJwas obtained for the proposed implementation when operated at an operating frequency of 100 MHz and load capacitance of 20 fF.MECRL also benefited from large power consumption by producing minimal power dissipation factor as low as 7.78 μW, much lower when compared to contemporary adiabatic logic inverter implementations. This output also denote the possibility of MECRL inverter to create a full adder and minimize the circuit's switchingspeed.

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